REMARKS

Claims 1 and 24 have been amended. Claim 1 has been amended in order to correct a typographical error. No new matter has been entered. Claims 1 - 25 are pending in this Application. Reconsideration and further examination is respectfully requested.

Allowable Subject Matter

1. The Applicants acknowledge the indication that claims 4 and 21 together with base and intervening claims define allowable subject matter.

Claim Rejections – 35 USC § 112

2. Claim 24 was rejected under 35 U.S.C. 112, 2nd paragraph, as being indefinite in that "said information units" lacked antecedent basis. Claim 24 has been amended to replace "information units" with "data units". The Applicants therefore respectfully request that this rejection be withdrawn.

Claim Rejections – 35 USC § 102

3. Claims 1, 2, 17, 18, and 25 were rejected under 35 U.S.C. 102(e) as being anticipated by Langevin et al. (U.S. Patent Publication 2003/0081548 A1). This rejection is respectfully traversed.

In accordance with the Applicants' invention, there is provided a communications switch having p inputs, q outputs, an ingress commutator, and an egress commutator. The switch of the Applicants' invention includes p+k buffer switches. An input data conditioner, comprising p inputs and p+k outputs, is coupled between the p inputs of the communications switch and the p+k information buffers. An output data conditioner comprising p+k inputs and q outputs is coupled between the p+k information buffers and the q outputs. The ingress commutator is operable to cyclically interconnect each of said p+k inputs of said input data conditioner to each of said p+k information buffers to provide data from said each of said p+k inputs of said input data conditioner to said p+k information storage buffers, said egress commutator operable to cyclically interconnect each of said p+k information storage buffers to said p+k inputs of said output data conditioner to provide data from said p inputs to said q outputs. One advantage of the claimed arrangement, as set forth in dependent claim 3, is that data can be transferred into the p+k storage buffers at a rate less than the rate at which data arrives at the p inputs.

A prima facie case of anticipation requires a showing of each and every element of the claim within the four corners of the cited reference. In rejecting claim 1, the Office Action refers to Fig. 10 of Langevin. Particularly, the Office Action refers to s0-s3 as representing inputs, d0-d3 as representing outputs, and t0,0 –t3,0 – t0,1-t3,1 as representing information storage buffers. Further elements of the Applicants' claims are not identified in particular, but generally by "see fig. 10, 0200".

Figure 10 of Langevin is a diagram of a fault tolerant version of a rotator switch as known in the art, wherein multiple physical paths are provided between an input and an output. (Langevin 0205). Upon further examination of Fig. 10, paragraph 200, and the rest of Langevin, the Applicants can find no teaching or suggestion of anything that might be considered an "input

data conditioner" or an "output data conditioner" as the Applicants have claimed. Because Langevin fails to teach or suggest the invention as set forth in Applicant's claim 1, the Applicants respectfully assert that Claim 1 and its dependent Claim 2 are in condition for allowance.

The Applicant's claim 17 sets forth "intermediate inputs" and intermediate outputs" whose functions are parallel to that of the data conditioners of claim 1. Langevin fails to teach or suggest these "intermediate inputs" and intermediate outputs" for the same reasons set forth with regard to the data conditioners of claim 1 above. The Applicants therefore respectfully assert that Claim 17 and its dependent Claim 18 are in condition for allowance.

The Applicant's Claim 25 sets forth "intermediate inputs" whose functions are parallel to that of the input data conditioner of Claim 1 and the intermediate inputs of Claim 17. Langevin fails to teach or suggest these "intermediate inputs" for the same reasons set forth with regard to the data conditioners of claim 1 and intermediate inputs of claim 17 above. The Applicants therefore respectfully assert that Claim 25 is in condition for allowance.

4. Claims 1 – 3, 5 – 20 and 22 – 25 were rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (2004/0085979 A1). This rejection is respectfully traversed.

In rejecting independent claims 1, 13, 17, and 25, the Office Action refers to Fig. 4 of Lee. Lee describes a crossbar switch scheduler for scheduling data transfers between input and output queues in a crossbar switch. Particularly, the Office Action refers to elements 10, 30 as representing the claimed "information storage buffers". The elements 10, 30 of Lee are input and output queues respectively. The Office Action then again refers to element 10, the input queue of Lee, as the claimed "input data conditioner". The office action then further directs

Applicants to "see fig. 4" for the claimed "ingress commutator for interconnecting each of said p+k information storage buffers to one of said p+k outputs of said input data conditioner". The Office Action's reference to any apparent "output data conditioner" in Lee appears to be in error. The Office Action generally recites Lee paragraphs 0029 – 0032 in support of the egress commutator claim language.

The Applicants disagree with the characterizations of Lee as set forth in the Office Action. The Applicants disagree that the input queue 10 of Lee, already characterized as the storage buffers, can then be properly characterized as the claimed "input data conditioner" of Claims 1 and 13, or the claimed "intermediate input" of Claims 17 and 25. The Applicants further disagree that Lee teaches or suggests the provision of an "ingress commutator" or "rotator switch" as the Applicants have claimed. The reference by the Office Action to fig. 4 of Lee fails to disclose any sort of input data conditioner having p+k outputs connected by any sort of commutator or rotator to information storage buffers, as claimed. Finally, no output data conditioner, intermediate output, or egress commutator is taught or suggested by Lee either.

Because Lee fails to teach or suggest all the elements of the invention as set forth in Applicant's independent Claims 1, 13, 17, and 25, the Applicants respectfully assert that Claims 1 – 3, 5 – 20 and 22 – 25 are in condition for allowance.

CONCLUSION

In view of the amendments and arguments made herein, Applicants submit that the application is in condition for allowance and request early favorable action by the Examiner.

If the Examiner believes that a telephone conversation with the Applicants' representative would expedite allowance of this application, the Examiner is cordially invited to call the undersigned at (508) 303-2003.

Respectfully submitted,

Date: September 27, 2007
Reg. No.: 37,946

/Mary M. Steubing/
Mary M. Steubing
Attorney for Applicants
Guerin & Rodriguez, LLP
5 Mount Royal Avenue
Marlborough, MA 01752

Fax No.: (508) 303-0005
Tel. No.: (508) 303-2003